REMARKS / ARGUMENTS

These remarks are responsive to the Office Action dated March 29, 2005. Claims 1-18 remain pending in the present application. Claims 1-12 are rejected. Claims 1, 3, 5, 6, 8, and 10 have been changed, and claims 13-19 have been added by this amendment.

Applicant has updated the Cross Related Applications section in the specification to indicate the serial numbers and patent numbers of the referenced patent applications.

The Examiner objected to claims 1, 3, 5-6, 8, and 10, stating that the recitation of "can be" and "can" are not positive recitations of the invention. Applicant has amended the claims to change these positive recitations as set forth above.

The 102 Rejections

The Examiner rejected claims 1-12 under 35 U.S.C. 102(e) as being anticipated by Payne et al., U.S. Patent No. 6,347,395 ("Payne"). Applicant respectfully traverses, and has amended the claims for clarification.

Payne discloses a silicon processing prototyping arrangement in which a reference chip development platform employs a collection of functional block macros to design a custom silicon chip. A functional prototype is validated on the platform and then the device is manufactured with a customer's requirements. External devices can be used to test a hardware representation of the functional block macros.

In contrast, Applicant recites a system on a chip in claim 1 that includes a plurality of logic functions including base functions and peripheral functions, and at least one field programmable

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gate array cell that is configurable to <u>selectively enable the peripheral functions in the field to allow</u> <u>access to the plurality of peripheral functions by a customer</u>. Payne discloses a development platform that can configure or deconfigure functional block macros for a chip <u>prototype</u> and include a customer's requirements in that prototype (col. 4, lines 30-47), but Payne mentions nothing about being able to configure and selectively enable peripheral functions in the field for a customer in a manufactured single chip. Payne's chip design has block macros that are configured for all chips manufactured based on that prototype chip design (reference chip), and assumes that each final, single-chip part is not configurable. Applicant's invention, however, allows selectively enabling particular peripheral functions in the field on the chip that the customer receives from the manufacturer, to allow access to those peripheral functions by the customer. Payne does not disclose or suggest any way for functionality to be enabled and configured in the field for manufactured system-on-a-chip in the field to allow access to those functions by a customer, thereby allowing one manufactured chip part to satisfy more than one product implementation. Furthermore, Payne's development system is a programmable chip coupled to one or more other external fixed logic chips, and is not a single system on a chip as in Applicant's claim.

Claims 2-5 are dependent from claim 1 and are believed patentable for at least the same reasons and for additional reasons.

Independent claims 6 and 10 recite SOC integrated circuits having pertinent features similar to those of claim 1, and are believed patentable for at least similar reasons as claim 1. Claims 7-9 and 11-12, respectively, are dependent from these independent claims and are patentable for at least similar reasons.

The Examiner rejected claims 1-12 under 35 U.S.C. 102(e) as being anticipated by Chen et al., U.S. Patent Pub. No. 2002/0010902 ("Chen"). Applicant respectfully traverses.

Chen discloses a field programmable gate array (FPGA) that has been adapted to be configured by all bitstream formats. An external processor interface allows direct access to embedded slave elements in the FPGA device.

Applicant's claim 1, however, recites a system on a chip in claim 1 that includes a plurality of logic functions including base functions and peripheral functions, and at least one FPGA cell that is configurable to selectively enable the peripheral functions in the field to allow access to the number of peripheral functions by a customer. Chen does not disclose or suggest an FPGA cell that can selectively enable peripheral functions in the field to allow access by the customer to those peripheral functions of a system on a chip; Chen is concerned with different formats of bit streams and external access to programmable functions on the chip.

Applicant therefore believes that claim 1 is patentable over Chen. Claims 2-5 are dependent from claim 1 and are believed patentable for at least the same reasons and for additional reasons. For example, Chen does not disclose or suggest an FPGA cell that is programmed to selectively complete connections from the bus to peripheral functions, or selectively tie the peripheral functions to an inactive state, as recited in claim 3.

Independent claims 6 and 10 recite SOC integrated circuits having pertinent features similar to those of claim 1, and are believed patentable for at least similar reasons as claim 1. Claim 10 also recites that the FPGA cell is programmed to selectively complete connections from one of the plurality of buses to the peripheral functions or selectively tie the peripheral functions to an inactive state, which is not disclosed or suggested by Chen. Claims 7-9 and 11-12, respectively,

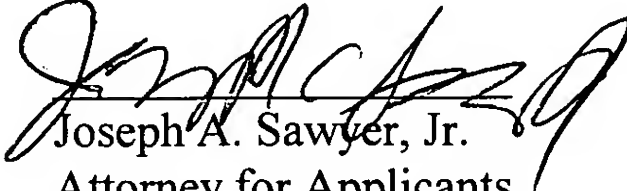are dependent from these independent claims and are patentable for at least similar reasons.

New claims

New claims 13-19 are dependent on claims 1, 6, and 10, and are patentable for at least the same reasons as these parent claims, and for additional reasons. For example, claims 13, 15, and 17 recites that the FPGA cell coupled to the plurality of peripheral functions is configured after power-on reset in a customer application, as disclosed in Applicant's specification on page 7, lines 19-23, and which is not disclosed or suggested by the cited references. Claims 14, 16, and 18 recite that the SOC integrated circuit is coupled to a companion ROM that stores a programming file that selectively enables the plurality of peripheral functions specific to the customer, as disclosed in Applicant's specification on page 7, lines 19-23, and which is not disclosed or suggested by the cited references. Claim 19 recites an enable status register coupled to at least one of the FPGA cells and allowing the determination of which peripheral functions are enabled after power-on reset before attempting to execute the peripheral functions, as disclosed in Applicant's specification on page 8, lines 15-21, and is not disclosed or suggested by the cited references.

In view of the remarks above, Applicant submits that the pending claims are patentable over Payne and respectfully requests that the rejection of claims 1-12 under 35 U.S.C. 102(e) be withdrawn and the pending claims 1-19 be allowed.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

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